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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,456	04/22/2005	Liberty L Gunter	20030213-US	3920

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EXAMINER
JEFFERSON, QUOVAUNDA

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/532,456	GUNTER ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10 and 12-14* is/are rejected.

7)☒ Claim(s) *2-8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 15-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on July 14th, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 9, 10, and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaudo et al, US Patent 6,156,581 in view of Kawai et al, US Patent 5,929,467, Romankiw, US Patent 4,224,361, Parikh et al, US Patent Application 2003/0015708 and Cheng et al, US Patent 5,215,619.

Regarding claim 1, Vaudo teaches a method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising of a hydride vapor phase

epitaxy (HVPE) grown n+ GaN quasi-substrate (column 6, lines 50-51, column 12, lines 51-60) and forming collector fingers **192**. Vaudo fails to teach opening a window for helium implantation on a GaN layer, using optical lithography, implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device, opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography, and etching to recess a base layer to an n- GaN layer grown on the n+ GaN layer, wherein the etching is performed with a ramp down in chuck bias voltage.

Vaudo fails to teach teaches opening a window for helium implantation on a GaN layer, using optical and implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device. However, Kawai teaches opening a window for helium implantation on a GaN layer, using optical lithography (column 4, lines 10-15 and column 5, lines 33-36) and implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads **17** (figure 5) of the device (column 5, lines 33-36 figure 8) because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai with that of Vaudo because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

Vaudo and Kawai fail to teach opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography; and etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage.

Romankiw teaches opening a window **50** for collector fingers using E-beam lithography **52,** depositing an ohmic metallization layer **25** over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers (figures 3a-3c and column 5, lines 22-30) as a simple, conventionally-known technique that is used to deposit metallic layers onto a substrate.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Romankiw with that of Vaudo and Kawai as a simple, conventionally known technique that is used to deposit metallic layers onto a substrate

Vaudo, Kawai, and Romankiw fail to teach opening a window for a self-aligned base recess using optical lithography; and etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage.

However, Parikh teaches opening a window for a self-aligned base recess using optical lithography and etching to recess a base layer to an n- GaN quasi-substrate layer **52** grown on the n+ GaN quasi-substrate layer **53** ([0049, 0004-0013] Note: Parikh teaches the use of a dry etch, RIE, to etch the base layer. It is well-known in the art that RIE etching uses a photoresist with an opening window that is used to designate in which areas the etching process is to take place) as a method of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Parikh with that of Vaudo, Kawai, and Romankiw as a method

of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

Vaudo, Kawai, Romankiw, and Parikh fails to teach the etching is performed with a ramp down in chuck bias voltage. However, Cheng teaches the etching is performed with a ramp down in chuck bias voltage (column 10, lines 5-12) when the magnetic field in the etching chamber is increased, which reduces the ion bombardment of the wafer and reduces device damage.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cheng with that of Vaudo, Kawai, Romankiw, and Parikh because decreasing the RF power and subsequent bias voltage reduces the ion bombardment of the wafer and reduces device damage.

Regarding claim 9, Parikh further teaches opening an emitter etch/contact window using optical lithography [0049] and the n+ GaN quasi-substrate layer. Parikh fail to teach etching an emitter recess to the quasi-substrate layer, depositing an emitter ohmic metallization layer over the etched emitter recess, and lifting-off emitter ohmic metallization, thereby forming an emitter contact pad. However, Romankiw further teaches etching an emitter recess to the quasi-substrate layer, depositing an emitter ohmic metallization layer over the etched emitter recess, and lifting-off emitter ohmic

metallization, thereby forming an emitter contact pad (figures 3a-3c and column 5, lines 22-30).

Regarding claim 10, Kawai further teaches the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold (column 4, lines 5-9).

Regarding claim 12, Vaudo, Kawai, Romankiw, Parikh, and Cheng fail to teach the helium implantation is achieved with an implant depth of about 2 μm. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 13, Romankiw further teaches the ohmic metallization layer over the window for the collector fingers is Ti/Ni (column 1, lines 60-67). Vaudo, Kawai, Romankiw, Parikh, and Cheng fail to teach the collector fingers with thicknesses of 100A and 400A, respectively. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 14, Vaudo further teaches the device has a plurality of collector fingers having a finger pitch between1: 1 and 1:3 (evenly spaced. See figure 15). Vaudo, Kawai, Romankiw, Parikh, and Cheng collector fingers about 0.2 μm wide. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

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data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh et al, US Patent Application 2003/0015708 in view of Cheng et al, US Patent 5,215,619.

Regarding claim 21, Parikh teaches a method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising of opening a window for a base recess ([0049] Note: Parikh teaches the use of a dry etch, RIE, to etch the base layer. It is well-known in the art that RIE etching uses a photoresist with an opening window that is used to designate in which areas the etching process is to take place); and etching to recess a base layer to an n- GaN quasi-substrate layer **53** grown on the n+ GaN quasi-substrate layer **52**. Parikh fails to teach the etching is performed with a ramp down in chuck bias voltage. However, Cheng teaches the etching is performed with a ramp down in chuck bias voltage (column 10, lines 5-12) when the magnetic field in the etching chamber is increased, which reduces the ion bombardment of the wafer and reduces device damage.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cheng with that of Parikh because decreasing the RF power and subsequent bias voltage reduces the ion bombardment of the wafer and reduces device damage.

Allowable Subject Matter

Claims 2-8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 2, prior art fails to teach depositing a high quality silicon nitride over the window layer for a collector contact pad, thereby forming a silicon nitride collector contact pad. Claims 3-6 are dependent upon claim 2, and are therefore allowable.

Regarding claim 7, prior art fails to teach depositing conformal silicon nitride **for** passivation of the recessed base layer, directionally etching to remove silicon nitride on planes parallel to the n+ GaN quasi-substrate layer, depositing a base metallization layer; and lifting-off base metallization, thereby forming a base contact pad. Claim 8 is dependent upon claim 7 and is therefore allowable.

Regarding claim 11, prior art fails to teach opening a window for RF test pad metallization using optical lithography, depositing an RF test pad metallization layer, and lifting-off RF test pad metallization, thereby providing RF test pads.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo
Patent Examiner
Art Unit 2823

QVJ

QVJ